

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Toshihiko TANAKA et al.

Appln. No.:

Filed: Herewith

For: METHOD OF MANUFACTURING AN ELECTRONIC DEVICE AND A
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants wish to make of record the documents cited
in prior Application No. 09/983,172 filed October 23, 2001,
whether cited by Applicants or by the Patent Office. The
documents are listed on the attached Form PTO-1449.

Respectfully submitted,

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October 15, 2003

By: 

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FORM PTO-1449				Atty. Docket No. XA-9566A		Appln. No.	
<u>LIST OF DOCUMENTS CITED BY APPLICANT</u>							
				Applicant Toshihiko TANAKA et al.			
				Filing Date HEREWITH		Group	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
FOREIGN PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL	9-211837	08/15/97	JAPAN			Abstract
	AM	5-289307	11/05/93	JAPAN			Abstract
	AN	5-181257	07/23/93	JAPAN			Abstract
	AO						
	AP						
	AQ						
OTHER (including author, title, date, pertinent pages, etc.)							
	AR						
	AS						
	AT						
Examiner				Date Considered			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							